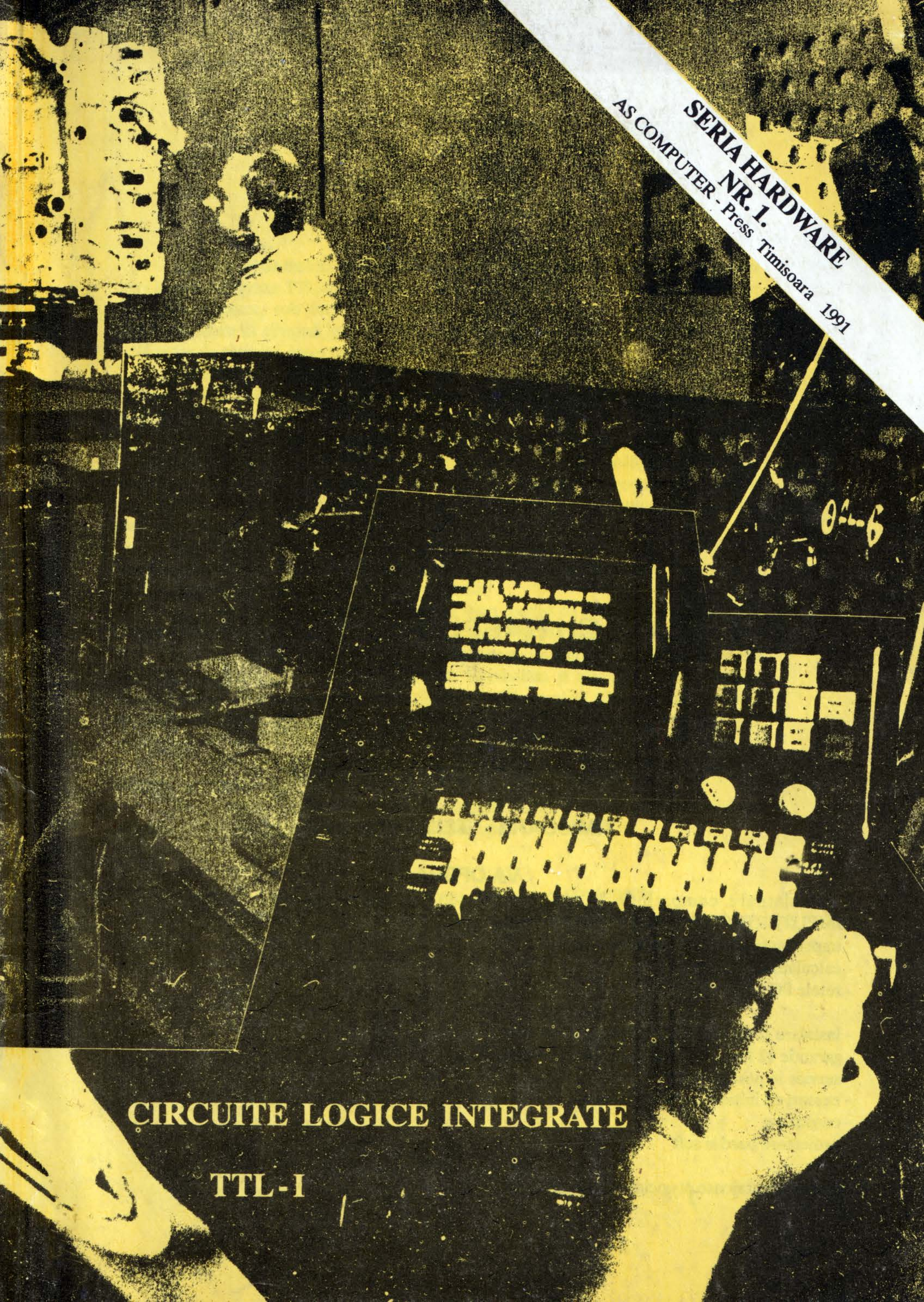


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CIRCUITE LOGICE INTEGRATE

TTL - I

PREFAȚĂ

Materialul de față își propune să vină în întîmpinarea numeroșilor utilizatori de circuite integrate TTL, CMOS sau ECL. În acest sens s-a considerat deosebit de utilă prezentarea, sub formă condensată, a unui catalog de astfel de circuite integrate, care să conțină informațiile esențiale pentru activitatea curentă a unui utilizator de circuite integrate numerice.

Selecția principalilor parametrii s-a făcut pe baza unei bogate experiențe didactice și practice, considerîndu-se că pentru marea majoritate a aplicațiilor un catalog condensat satisface cerințele utilizatorilor.

Pentru întocmirea catalogului condensat s-au studiat un număr important de cataloage și date tehnice furnizate de principalele firme producătoare de circuite integrate. S-a încercat totodată, o prezentare a acestui compendiu de circuite integrate într-un mod cît mai unitar, fără a neglija unele particularități specifice anumitor tipuri de circuite integrate numerice.

Catalogul condensat care urmează a fi prezentat în mai multe fascicole, v-a conține toată gama de circuite integrate numerice din cadrul familiilor TTL, CMOS și ECL, existente în prezent pe piața mondială.

În primul fascicol se vor prezenta pe scurt modul de definire a parametrilor circuitelor integrate cît și primele 100 de tipuri de circuite integrate TTL.

În următoarele se va continua cu prezentarea următoarelor 700 de tipuri de circuite integrate TTL, intenționînd ca să intercalăm și unele aspecte specifice acestei familii de circuite integrate, astfel încît utilizatorul să aibă o viziune cît mai completă asupra avantajelor și eventualelor dezavantaje pe care le implică realizarea unor sisteme numerice folosind astfel de circuite.

În mod asemănător ne propunem abordarea și celorlalte două familii de circuite integrate CMOS și ECL.

Seria prezentărilor celor mai importante circuite integrate numerice se dorește să se termine cu o selecție de aplicații utile.

Coordonator
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grafica Popa'S

1.Parametrii circuitelor logice integrate (CLI)

Parametrii circuitelor logice integrate precizeaza regulile de interconectare si caracterizeaza performantele pe care le prezinta acestea.

In functie de schema electronica si aparitia cronologica C L I se impart in familii de circuite integrate. Circuitele dintr-o familie prezinta aceleasi nivele logice si sint caracterizate prin parametrii definiti identici.

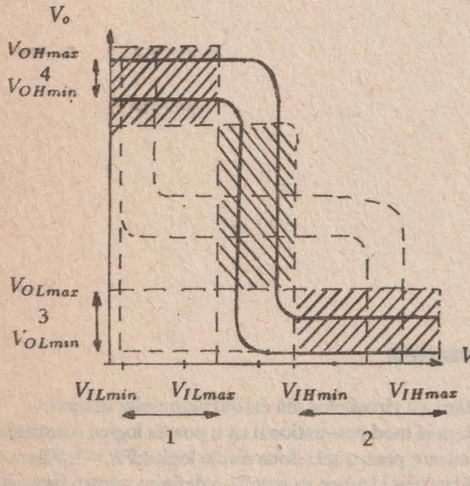
La rindul lor o familie de CLI poate fi clasificata in "serii de CLI". Fiecare serie se remarca prin performante sporite a unui parametru; fiind denumita dupa parametrul respectiv.

Din punct de vedere electric un CLI se caracterizeaza prin urmatorii parametrii: tensiunea de alimentare, nivele logice de tensiune, puterea consumata, viteza, protectia contra zgomotelor, curentii de intrare si iesire, parametrii ce caracterizeaza regulile de interconectare.

1.1. Caracteristica statica de transfer

Caracteristica statica de transfer a unui CLI reprezinta variatia tensiunii de iesire functie de tensiunea de intrare. Datorita variatiei tensiunii de alimentare, a parametrilor componentelor semiconductoare si temperaturilor de lucru diferite, pentru o familie de CLI sint valabile caracteristici limita de transfer (fig.1). Pe baza caracteristicilor din fig.1 se pot defini variabilele logice.

Astfel fiecare variabila logica se asociaza la doua plaje de tensiune : plaja tensiunilor garantate la iesire si plaja tensiunilor admise la intrare.Un CLI functioneaza corect, din punct de vedere logic, daca toate tensiunile de intrare sint plasate in una din plajele admise, ceea ce determina ca tensiunea de iesire sa se gaseasca in plaja garantata corespunzatoare tensiunii de iesire. Cele patru plaje de tensiune sint delimitate de opt tensiuni limita:



1.Plaja admisa la intrare pentru "0" logic V_{iLmax}-V_{iLmin}

2.Plaja admisa la intrare pentru "1" logic V_{iHmax}-V_{iHmin}

3.Plaja garantata la iesire pentru "0" logic V_{0Lmax}-V_{iLmin}

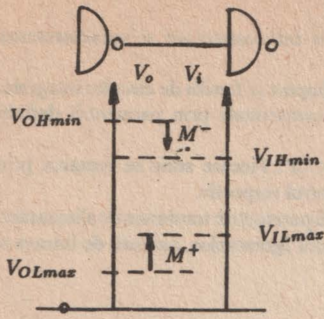
3.Plaja garantata la iesire pentru "1" logic V_{0Hmax}-V_{iHmin}

Fig. 1

1.2. Marginea de protectie contra perturbatiilor

Marginea de protectie contra semnalelor perturbatoare, numita si imunitate la zgomot a unui CLI, este egala cu valoarea maxima pe care o poate lua tensiunea perturbatoare la intrarea circuitului, astfel ca la iesirea acestuia sa se mentina nivelul de tensiune in cadrul plajei garantate. Intr-un sistem numeric fiecare circuit este actionat de alt circuit si la rindul lui comanda un circuit.

Definirea marginii de zgomot se face ca in fig.2.

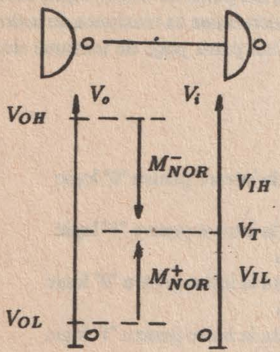


$M^+ = V_{iLmax} - V_{0Lmax}$

$M^- = V_{0Hmin} - V_{iHmin}$

Fig. 2

Marimile definite mai sus prezinta valori minime. Daca se apreciaza ca sistemul numeric, ce utilizeaza CLI nu lucreaza in conditii deosebit de defavorabile atunci se poate defini o margine de zgomot normala (fig.3).



$M^+_{NOR.} = V_T - V_{0L}$
$M^-_{NOR.} = V_{0H} - V_T$

unde V_T reprezinta tensiunea de prag

Fig. 3

1.3. Factorul de incarcare

Acest parametru defineste regulile de interconectare ale circuitelor din cadrul sistemului numeric.

Pentru definirea factorului de incarcare se considera in mod conventional ca o poarta logica constituie sarcina unitara; definind factorul de incarcare la intrare pentru cele doua nivele logice: $FI_L = 1$; $FI_H = 1$

Considerind ca un circuit logic va comanda alte N circuite identice va rezulta o definire pentru factorul de incarcare la iesire in cele doua situatii

$$FE_H = \left| \frac{I_{0H}}{I_{iH}} \right| \qquad FE_L = \left| \frac{I_{0L}}{I_{iL}} \right|$$

Se poate constata ca cei patru factori de incarcare sint numere intregi pozitive.

Se precizeaza ca toti curentii de intrare/iesire au semnale pozitive daca sint absorbiti de CLI (spre circuit) in caz contrar se atribuie,in mod conventional, semnul negativ.

Daca circuitele logice interconectate prezinta curenti de intrare/iesire diferiti se impune respectarea urmatoarelor relatii: $I_{0H} = \Sigma I_{iH}$; $I_{0L} = \Sigma I_{iL}$

1.4. Puterea consumata

Acest parametru defineste puterea absorbita de CLI de la sursa de alimentare.

Parametrul are trei componente:

Puterea consumata in regim static :

$$Pcc = \frac{I_{CCH} + I_{CCL}}{2} Vcc$$

unde curentii I_{CC} sint curenti absorbiti de la sursa de alimentare in regim static atunci cind la iesire este "1" respectiv "0" logic.

Puterea consumata in regim dinamic :

$$P_{d1} = Vcc^2 \; Cp.f$$

unde:

Vcc - tensiunea de alimentare.

Cp - capacitatile parazite de la iesirea CLI.

f - frecventa de lucru a CLI.

P_{d2} - puterea dinamica datorata supracurentilor rezultati in urma comutarii si care depind de schema interna a CLI.

1.5. Viteza de comutare

Este parametrul ce specifica frecventa maxima de lucru a CLI cit si timpul de raspuns al acestuia din momentul aplicarii semnalului de intrare. Timpul de raspuns al CLI poarta denumirea de timp de propagare si este definit ca in fig.4

$$tpd = \frac{tpHL + tpLH}{2}$$

unde tpd - timpul de propagare mediu.

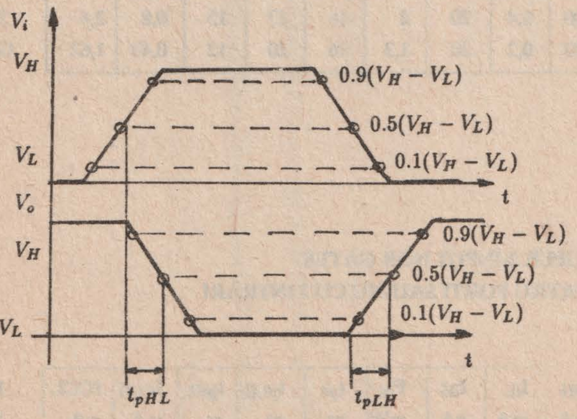


Fig. 4

1.6. Factorul de calitate

Constitue produsul dintre puterea statica si timpul de propagare mediu.

7400 QUADRUPLE 2-INPUT NAND GATES

$V_{cc} = 5V$ PATRU PORTI SI-NU CU 2 INTRARI

Y = [illegible]

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} μA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
00	16	0,8	1,6	40	10	10	11	7	4	12
LS00	8	0,4	0,4	20	2	9,5	9	10	0,8	2,4
S00	20	1	2	50	19	3	3	3	10	20
ALS00	8	0,4	0,2	20	1,3	4,5	4	5	0,43	1,62
L00	3,6	0,2	0,18	10	1	33	35	31	0,44	1,16
H00	20	1	2	50	22	6	5,9	6,2	10	26

1A	1	14	Vcc
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7401 QUADRUPLE 2-INPUT NAND GATES WITH OPEN COLLECTORS OUTPUTS

$V_{cc} = 5V$ PATRU PORTI SI-NU CU 2 INTRARI CU COLECTOR IN GOL

Y = [illegible]

TIP 74	I_{OL} mA	I_{OH} μA	I_{iL} mA	I_{iH} μA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
01	16	250	1,6	40	10	22	35	8	4	12
H01	20	250	2	50	20,5	9	10	7,5	10	26
L01	3,6	50	0,18	10	1	47	60	33	0,44	1,16
LS01	8	100	0,4	20	2	16	17	15	0,8	2,4
ALS01	8	100	0,2	20	1,3	16	20	12	0,43	1,62

1Y	1	14	Vcc
1A	2	13	4Y
1B	3	12	4B
2Y	4	11	4A
2A	5	10	3Y
2B	6	9	3B
GND	7	8	3A

7402 QUADRUPLE 2-INPUT NOR GATES

$V_{cc} = 5V$ PATRU PORTI SAU-NU CU 2 INTRARI

Y = [illegible]

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} μA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	ICCL mA
02	16	0,4	1,6	40	14	10	12	8	8	14
L02	3,6	0,1	0,18	10	1,4	33	31	35	0,8	1,4
LS02	8	0,4	0,4	20	2,8	10	10	10	1,6	2,8
S02	20	1	2	50	29	3,5	3,5	3,5	17	26,26
ALS02	8	0,4	0,4	20	1,9	5,5	6	5	0,86	2,16

1Y	1	14	Vcc
1A	2	13	4Y
1B	3	12	4B
2Y	4	11	4A
2A	5	10	3Y
2B	6	9	3B
GND	7	8	3A

7403 QUADRUPLE 2-INPUT NAND GATES WITH OPEN COLLECTOR OUTPUTS

Vcc = 5V PATRU PORTI SI-NU CU 2 INTRARI CU COLECTOR IN GOL

Y

TIP 74	I_{0L} mA	I_{0H} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
03	16	250	1,6	40	10	22	35	8	4	12
LS03	8	100	0,4	20	2	16	17	15	0,8	2,4
S03	20	250	2	50	17,5	5	5	4,5	6	20
ALS03	8	100	0,2	20	1,25	16	20	12	0,43	1,63
L03	3,6	50	0,18	10	1	46	60	33	0,44	1,16

1A	1	14	Vcc
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7404 HEX INVERTERS

Vcc = 5V SASE INVERTOARE

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
04	16	0,4	1,6	40	10	10	12	8	6	18
LS04	8	0,4	0,4	20	2	9,5	9	10	1,2	3,6
S04	20	1	2	50	19	3	3	3	15	30
ALS04	8	0,4	0,2	20	1,25	3,5	3,5	3,5	0,65	2,4
H04	20	1	2	50	22	6	6	6,5	16	40
L04	3,6	0,2	0,18	10	1	33	35	31	0,66	1,74

1A	1	14	Vcc
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

7405 HEX INVERTERS WITH OPEN COLLECTOR OUTPUTS

Vcc = 5V SASE INVERTOARE CU COLECTOR IN GOL

Y

TIP 74	I_{0L} mA	I_{0H} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCL} mA	I_{CCH} mA
05	16	250	1,6	40	10	24	40	8	6	18
LS05	8	100	0,4	20	2	16	17	15	1,2	3,6
S05	20	250	2	50	17,5	5	5	4,5	9	30
ALS05	8	100	0,2	20	1,25	14	20	7	0,65	2,4
H05	20	250	2	50	23,4	9	10	7,5	16	40

1A	1	14	Vcc
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

7406 HEX INVERTERS BUFFERS/DRIVERS WITH OPEN COLLECTOR HIGH-VOLTAGE OUTPU

Vcc = 5V 6 INVERTOARE CU COLECTOR IN GOL DE TENSIUNE RIDICATA

$Y = \overline{A}$; V0H = 30V

TIP 74	I_{0L} mA	I_{0H} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
06	40	250	1,6	40	26	12,5	10	15	30	32

IDENTIC CU 7405

7407 HEX BUFFERS/DRIVERS WITH OPEN COLLECTOR HIGH-VOLTAGE OUTPUTS

Vcc = 5V 6 CIRCUITE DE COMANDA CU COLECTOR IN GOL SI DE TENSIUNE RIDICATA

Y = A ; V0H = 30V

TIP 74	I_{0L} mA	I_{0H} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
07	40	250	1,6	40	21	13	6	20	29	21

1A	1	14	Vcc
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

7408 QUADRUPLE 2-INPUT AND GATES

Vcc = 5V PATRU PORTI SI CU 2 INTRARI

Y = A.B

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
08	16	0,8	1,6	40	19	15	17,5	12	11	20
LS08	8	0,4	0,4	20	4,3	12	8	10	2,4	4,4
S08	20	1	2	50	32	4,8	4,5	5	18	32
ALS08	8	0,4	0,2	20	2,2	6,5	8	5	1,3	2,2

1A	1	14	Vcc
1B	2	11	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7409 QUADRUPLE 2-INPUT AND GATES WITH OPEN COLLECTOR

Vcc = 5V PATRU PORTI SI CU 2 INTRARI SI COLECTOR IN GOL

Y = A.B ; V0H = 5V

TIP 74	I_{0L} mA	I_{0H} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
09	16	250	1,6	40	19,5	18,5	21	16	11	20
LS09	8	100	0,4	20	4,3	18,5	20	17	2,4	4,4
S09	20	250	2	50	32	6	5,5	6	18	32
ALS09	8	100	0,2	20	2,2	15	20	10	1,35	2,2

1A	1	14	Vcc
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7410 TRIPLE 3-INPUT-NAND GATES

$V_{cc}=5V$ TREI CIRCUITE SI-NU CU 3 INTRARI

$Y=\overline{A.B.C}$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} μA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
10	16	0,4	1,6	40	10	10	11	7	3	9
H10	20	0,5	2	50	22,5	6	5,9	6,3	7,5	19,5
L10	3,6	0,2	0,18	10	1	33	35	31	0,33	0,87
LS10	8	0,4	0,4	20	2	9,5	9	10	0,6	1,8
S10	20	1	2	50	19	3	3	3	7,5	1,5
ALS10	8	0,4	0,2	20	1,25	7	4	10	0,32	1,2

1A	1	14	Vcc
1B	2	13	1C
2A	3	12	1Y
2B	4	11	3C
2C	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7411 TRIPLE 3-INPUT-AND GATES

$V_{cc}=5V$ TREI PORTI SI CU 3 INTRARI

$Y= A.B.C$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} μA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
H11	20	0,5	2	50	40	8,2	7,6	8,8	18	30
LS11	8	0,4	0,4	20	4,3	9	8	10	1,8	3,3
S11	20	1	2	50	31	4,8	4,5	5	13,5	24
ALS11	8	0,4	0,2	20	2,2	9	12	6	1	1,6

1A	1	14	Vcc
1B	2	13	1C
2A	3	12	1Y
2B	4	11	3C
2C	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7412 TRIPLE 3-INPUT-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

$V_{cc}=5V$ TREI CIRCUITE SI-NU CU TREI INTRARI CU COLECTORUL IN GOL

$Y=\overline{A.B.C}$; $V_{OH}=5V$

TIP 74	I_{OL} mA	I_{OH} μA	I_{iL} mA	I_{iH} μA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
12	16	250	1,6	40	10	22	35	8	3	9
LS12	8	100	0,4	20	2	16	17	15	0,7	1,8
ALS12	8	100	0,2	20	1,25	18	20	15	0,32	1,2

1A	1	14	Vcc
1B	2	13	1C
2A	3	12	1Y
2B	4	11	3C
2C	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7413 DUAL FOUR INPUT NAND SCHMITT TRIGGER

Vcc = 5V DOUA TRIGGERE SCHMITT SI-NU CU PATRU INTRARI

$Y = \overline{A.B.C.D}$; $V_{T+} = 1{,}7V$; $V_{T-} = 0{,}9V$

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} uA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
13	16	0,8	1,6	40	42	16,5	18	15	14	20
LS13	8	0,4	0,4	20	9	16,5	15	18	2,9	4,1

1A	1	14	Vcc
1B	2	13	2D
	3	12	2C
1C	4	11	
1D	5	10	2B
1Y	6	9	2A
GND	7	8	2Y

7414 HEX SCHMITT-TRIGGER INVERTERS

Vcc = 5V SASE INVERSOARE TRIGGER-SCHMITT

$Y = \overline{A}$; $V_{T+} = 1{,}7V$; $V_{T-} = 0{,}9V$

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} uA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
14	16	0,8	1,2	40	26	15	15	15	22	39
LS14	8	0,4	0,4	20	8,6	15	15	15	8,6	12

1A	1	14	Vcc
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

7415 TRIPLE 3-INPUT-AND GATES WITH OPEN COLLECTOR OUTPUTS

Vcc = 5V TREI PORTI SI CU TREI INTRARI CU COLECTOR IN GOL

$Y = A.B.C$; $V_{OH} = 5V$

TIP 74	I_{0L} mA	I_{0H} uA	I_{iL} mA	I_{iH} uA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
H15	20	250	2	50	37,5	11	12	9	15	30
LS15	8	100	0,4	20	4,3	19	20	17	1,8	3,3
S15	20	250	2	50	28	6	5,5	6	10,5	24
ALS15	8	100	0,2	20	2,25	15	20	10	1	1,66

1A	1	14	Vcc
1B	2	13	1C
2A	3	12	1Y
2B	4	11	3C
2C	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7416 HEX INVERTER BUFFERS/DRIVERS WITH OPEN COLLECTOR HIGH-VOLTAGE OUTPUTS

Vcc = 5V SASE INVERTOARE DE COMANDA CU COLECTOR IN GOL CU TENSIUNE RIDICATA L IESIRE

$Y = \overline{A}$, $V_{OH} = 15V$

TIP 74	I_{0L} mA	I_{0H} uA	I_{iL} mA	I_{iH} uA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
16	40	250	1,6	40	26	12,5	10	15	30	32

IDENTIC CU 7404

7417 HEX BUFFERS/DRIVERS WITH OPEN COLLECTOR HIGH-VOLTAGE OUTPUTS

Vcc = 5V SASE CIRCUITE DE COMANDA CU COLECTOR IN GOL SI DE TENSIUNE RIDICATA IESIRE

Y = A ; V0H = 15V

TIP 74	I_{0L} mA	I_{0H} uA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
17	40	250	1,6	40	21	13	6	20	29	21

IDENTIC CU 7407

7418 DUAL FOUR INPUT NAND SCHMITT-TRIGGER

Vcc = 5V DOUA TRIGGERE SCHMITT SI-NU CU PATRU INTRARI

Y = A.B.C.D ; VT+ = 1,6V ; VT- = 0,8V

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
LS18	8	0,4	0,4	20	9	17	15	18	2,9	4,1

IDENTIC CU 7413

7419 HEX SCHMITT TRIGGER INVERTERS

Vc = 5V SASE INVERTOARE TRIGGERE SCHMITT

Y = $\overline{A}$; VT+ = 1,6V ; VT- = 0,8V

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
LS19	8	0,4	0,4	20	8,6	15	15	15	8,6	12

IDENTIC CU 7414

7420 DUAL 4-INPUT NAND GATES

Vcc = 5V DOUA PORTI SI-NU CU PATRU INTRARI

Y = $\overline{A.B.C.D}$

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
20	16	0,4	1,6	40	10	10	12	8	2	6
LS20	8	0,4	0,4	20	2	9,5	9	10	0,4	1,2
S20	20	1	2	50	19	3	3	3	5	10
ALS20	8	0,4	0,2	20	1,25	9,5	4	15	0,22	0,81
H20	20	0,5	2	50	22,5	6,5	6	7	5	13
L20	2	0,2	0,18	10	1	33	35	31	0,22	0,58

1A	1	14	Vcc
1B	2	13	2D
	3	12	2C
1C	4	11	
1D	5	10	2B
1Y	6	9	2A
GND	7	8	2Y

7421 DUAL 4-INPUT AND GATES

Vcc = 5V DOUA PORTI SI-NU CU 4 INTRARI

$Y = A.B.C.D$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
LS21	8	0,4	0,4	20	4,3	9	8	10	1,2	2,2
ALS21	8	0,4	0,4	20	2,25	8,5	12	5	0,67	1,1
H21	20	0,5	2	50	40	8,2	7,6	8,8	12	20

1A	1	14	Vcc
1B	2	13	2D
	3	12	2C
1C	4	11	
1D	5	10	2B
1Y	6	9	2A
GND	7	8	2Y

7422 DUAL 4-INPUT NAND GATES WITH OPEN-COLLECTOR OUTPUTS

Vcc = 5V DOUA PORTI SI-NU CU 4 INTRARI SI COLECTOR IN GOL

$Y = \overline{A.B.C.D}$; V0H = 5V

TIP 74	I_{OL} mA	I_{OH} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
22	16	250	1,6	40	10	22	35	8	2	6
LS22	8	100	0,4	20	2	16	17	15	0,4	1,2
S22	20	250	2	50	16,2	5	5	4,5	3	10
ALS22	8	100	0,2	20	1,25	20	20	19	0,22	0,8
H22	20	250	2	50	20,5	9	10	7,5	0,5	13

1A	1	14	Vcc
1B	2	13	2D
	3	12	2C
1C	4	11	
1D	5	10	2B
1Y	6	9	2A
GND	7	8	2Y

7423 EXPANDABLE DUAL 4-INPUT NOR GATES WITH STROBE

Vcc = 5V DOUA PORTI SAU-NU EXPANDABILE CU 4 INTRARI SI CU STROBARE

$1Y = \overline{1G(1A+1B+1C+1D)+X}$; X = OUTPUT OF 7460

$2Y = \overline{2G(2A+2B+2C+2D)}$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
23	16	0,8	1,6	40	23	10,5	13	8	8	10
STROBE G			6,4	160						

1X	1	16	Vcc
1A	2	15	$\overline{1X}$
1B	3	14	2D
1G	4	13	2C
1C	5	12	2G
1D	6	11	2B
1Y	7	10	2A
GND	8	9	2Y

7424 QUADRUPLE 2 INPUT NAND SCHMITT TRIGGER

Vcc = 5V PATRU TRIGGERE SCHMITT SI-NU CU 2 INTRARI

$Y = A.B$; VT+ = 1,6V ; VT- = 0,8V

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
LS24	8	0,4	0,4	20	8,5	16	15	17	5,4	8

IDENTIC CU 7400

7425 DUAL 4-INPUT NOR GATES WITH STROBE

Vcc=5V DOUA PORTI SAU-NU CU 4 INTRARI SI CU STROBARE

$Y=\overline{G(A+B+C+D)}$

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} uA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
25	16	0,8	1,6	40	23	10,5	13	8	8	10
STROB G			6,4	160						

1A	1	14	Vcc
1B	2	13	2D
1G	3	12	2C
1C	4	11	2G
1D	5	10	2B
1Y	6	9	2D
GND	7	8	2Y

7426 QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE NAND GATES

Vcc=5V PATRU PORTI SI-NU CU 2 INTRARI CU COLECTOR IN GOL

$Y=\overline{A.B}$; V0H=15V

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
26	16	1	1,6	40	10	13,5	16	11	4	12
LS26	8	1	0,4	20	2	16	17	15	0,8	2,4

IDENTIC CU 7400

7427 TRIPLE 3-INPUT NOR GATES

Vcc=5V TREI PORTI SAU-NU CU TREI INTRARI

$Y=\overline{A+B+C}$

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	Pcc mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
27	16	0,8	1,6	40	22	8,5	10	7	10	16
LS27	8	0,4	0,4	20	4,5	10	10	10	2	3,4
ALS27	8	0,4	0,2	20	2,5	6	9	3	0,97	2

1A	1	14	Vcc
1B	2	13	1C
2A	3	12	1Y
2B	4	11	3C
2C	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7428 QUADRUPLE 2-INPUT NOR GATES

Vcc=5V PATRU PORTISAU-NU CU 2 INTRARI

$Y=\overline{A+B}$

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
28	48	2,4	1,6	40	28	7	6	8	12	33
LS28	24	1,2	0,4	20	5,5	12	12	12	1,8	6,9
ALS28	24	2,6	0,2	20	4	4	4	4	1,7	4,8

IDENTIC CU 7402

7430 8-INPUT NAND GATES

Vcc=5V POARTA SI-NU CU 8 INTRARI

$Y=\overline{A.B.C.D.E.F.G.H}$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
30	16	0,4	1,6	40	10	11	13	8	1	3
LS30	8	0,4	0,4	20	2,4	11	8	13	0,35	0,6
S30	20	1	2	50	21	4	4	4,5	3	5,5
ALS30	8	0,4	0,2	20	1,9	7	4	10	0,22	0,54
H30	20	0,5	2	50	22,5	7,9	6,8	8,9	2,5	6,56
L30	3,6	0,2	0,18	20	1	53	35	70	0,11	0,29

A	1	14	Vcc
B	2	13	
C	3	12	H
D	4	11	G
E	5	10	
F	6	9	
GND	7	8	Y

7432 QUADRUPLE 2-INPUT OR GATES

Vcc=5V PATRU PORTI SAU CU 2 INTRARI

$Y=\overline{A+B}$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
32	16	0,8	1,6	40	24	12	10	14	15	23
LS32	8	0,4	0,4	20	5	14	14	14	3,1	4,9
S32	20	1	2	50	35	4	4	4	18	38
ALS32	8	0,4	0,4	20	2,8	5,5	6	5	1,9	2,6

1A	1	14	Vcc
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3Y
2Y	6	9	3A
GND	7	8	3Y

7433 QUADRUPLE 2-INPUT NOR BUFFERS WITH OPEN COLLECTOR OUTPUTS

Vcc=5V PATRU PORTI SAU-NU CU 2 INTRARI DE PUTERE CU COLECTOR IN GOL

$Y=\overline{A+B}$; $V_{OH}=5V$

TIP 74	I_{OL} mA	I_{OH} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
33	48	250	1,6	40	28	11	10	12	12	33
LS33	24	250	0,4	20	5,5	19	20	18	1,8	6,9
ALS33	24	100	0,2	20	4	14	20	9	1,7	4,8

1Y	1	14	Vcc
1A	2	13	4Y
1B	3	12	4B
2Y	4	11	4A
2A	5	10	3B
2B	6	9	3B
GND	7	8	3A

7437 QUADRUPLE 2-INPUT NAND BUFFERS

Vcc=5V PATRU PORTI SI-NU CU 2 INTRARI DE PUTERE

$Y=\overline{A.B}$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
37	48	1,2	1,2	40	27	10	13	8	9	34
LS37	24	1,2	0,4	20	4,3	12	12	12	0,9	6
S37	60	3	4	100	41	4	4	4	20	46
ALS37	24	2,6	0,2	20	3	4	4	4	0,86	4

1A	1	14	Vcc
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7438 QUADRUPLE 2-INPUT NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

Vcc=5V PATRU PORTI SI-NU CU 2 INTRARI DE PUTERE CU COLECTOR IN GOL

$Y=\overline{A.B}$; $V_{0H}=5V$

TIP 74	I_{0L} mA	I_{0H} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
38	48	250	1,6	40	24,5	12,5	14	11	5	34
LS38	24	250	0,4	20	4,3	19	20	18	0,9	6
S38	60	250	4	100	41	6,5	6,5	6,5	20	46
ALS38	24	100	0,2	20	3	14,5	20	9	0,86	4

1A	1	14	Vcc
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7440 DUAL 4-INPUT NAND BUFFERS

Vcc=5V DOUA PORTI SI-NU CU 4-INTRARI DE PUTERE

$Y=\overline{A.B}$

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} uA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
40	48	1,2	1,6	40	26	10,5	13	8	4	17
LS40	24	1,2	0,4	20	4,3	12	12	12	0,45	3
S40	60	3	4	100	44	6	6	6	10	25
ALS40	24	2,6	0,2	20	3	4	4	4	0,43	2
H40	60	1,5	4	100	44	7,5	8,5	6,5	10,5	25

1A	1	14	Vcc
1B	2	13	2D
	3	12	2C
1C	4	11	
1D	5	10	2B
1Y	6	9	2A
GND	7	8	2Y

7442 4-LINE-TO-10-LINE DECODERS/BCD-TO-DECIMAL

Vcc=5V DECODIFICATOR 4 IN 10/BCD-ZECIMAL

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	I_{cc} mA	t_{pd} ns	t_{pHL} ns	t_{pLH} ns
42A	16	0,8	1,6	40	140	28	17	17	17
L42	8	0,4	0,8	20	70	14	49	46	52
LS42	8	0,4	0,4	20	35	7	20	20	20

No	BCD-INPUT		DECIMAL-OUTPUT				
	DC	BA	01	23	45	67	89
0	LL	LL	LH	HH	HH	HH	HH
1	LL	LH	HL	HH	HH	HH	HH
2	LL	HL	HH	LH	HH	HH	HH
3	LL	HH	HH	HL	HH	HH	HH
4	LH	LL	HH	HH	LH	HH	HH
5	LH	LH	HH	HH	HL	HH	HH
6	LH	HL	HH	HH	HH	LH	HH
7	LH	HH	HH	HH	HH	HL	HH
8	HL	LL	HH	HH	HH	HH	LH
9	HL	LH	HH	HH	HH	HH	HL
10-15	HX	XX	HH	HH	HH	HH	HH

0	1	16	Vcc
1	2	15	A
2	3	14	B
3	4	13	C
4	5	12	D
5	6	11	9
6	7	10	8
GND	8	9	7

X = L/H

7443 4-LINE-TO-10-LINE DECODERS/EXCESS-3-TO-DECIMAL

Vcc = 5V DECODIFICATOR 4 IN 10/EXCES DE 3-ZECIMAL

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} μA	P_{cc} mW	I_{cc} mA	t_{pd} ns	t_{pHL} ns	t_{pLH} ns	TIP 74
43A	16	0,8	1,6	40	140	28	17	17	1	44A
L43	8	0,4	0,8	20	70	14	49	46	52	L44

IDENTIC CU 7442

No	7443 EX.3-INPUT		DECIMAL-OUTPUT					7444 EX.3 GRAY-IN.		
	AB	CD	01	23	45	67	89	AB	C	D
0	LL	HH	LH	HH	HH	HH	HH	LL	H	L
1	LH	LL	HL	HH	HH	HH	HH	LH	H	L
2	LH	LH	HH	LH	HH	HH	HH	LH	H	H
3	LH	HL	HH	HL	HH	HH	HH	LH	L	H
4	LH	HH	HH	HH	LH	HH	HH	LH	L	L
5	HL	LL	HH	HH	HL	HH	HH	HH	L	L
6	HL	LH	HH	HH	HH	LH	HH	HH	L	H
7	HL	HL	HH	HH	HH	HL	HH	HH	H	H
8	HL	HH	HH	HH	HH	HH	LH	HH	H	L
9	HH	LL	HH	HH	HH	HH	HL	HL	H	L
10-15	XX	XX	HH	HH	HH	HH	HH	XX	X	X

X = H/L

7444 4-LINE-TO-10-LINE DECODERS/EXCESS-3 GRAY-TO DECIMAL

DECODIFICATOR 4 IN 10/EX-3 GRAY-ZECIMAL

VEZI 7443

7445 BCD-TO-DECIMAL DECODER/DRIVER

$V_{cc} = 5V$ DECODIFICATOR DE PUTERE /IESIREA IN GOL ; $V_{OH} = 30V$

TIP 74	I_{OL} mA	I_{OH} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	I_{cc} mA	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
45	80	250	1,6	40	215	43	50	50	50

DISPUNEREA PINILOR SI TABELA DE FUNCTII IDENTIC CU 7442

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

7446 ACTIVE-LOW,OPEN-COLLECTOR,30V OUTPUTS

7447 ACTIVE-LOW,OPEN-COLLECTOR,15V OUTPUTS

7448 INTERNAL PULL-UP-OUTPUTS

7449 OPEN COLLECTOR OUTPUTS

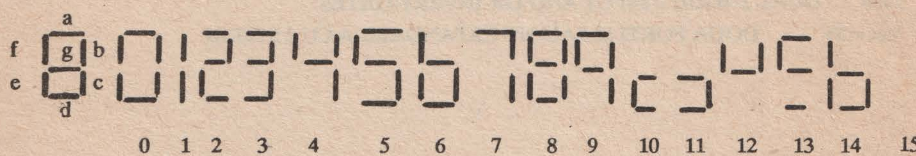
$V_{cc} = 5V$ DECODIFICATOARE DE PUTERE/BCD-7 SEGMENTE

TIP 74	I_{OL} mA	I_{OH} µA	$I_{O(on)}$ mA	$I_{O(off)}$ µA	P_{cc} mW	I_{cc} mA	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	V_{OH} V
46A	8	200	40	250	320	64	100	100	100	30
L46	4	100	20	250	160	32	200	200	200	30
47A	8	200	40	250	320	64	100	100	100	15
L47	4	100	20	250	160	32	200	200	200	15
LS47	3,2	50	24	250	35	7	100	100	100	15
48	8	200	6,4	400	265	53	100	100	100	5
LS48	3,2	50	6	100	125	25	100	100	100	5
49	10	250	-	-	165	33	100	100	100	5
LS49	8	250	-	-	40	8	100	100	100	5

SEGMENTE

7446
7447
7448

B	1	16	Vcc
C	2	15	f
LT	3	14	g
RBo	4	13	a
RBI	5	12	b
D	6	11	c
A	7	10	d
GND	8	9	e



7449

B	1	14	Vcc
C	2	13	f
BI	3	12	g
D	4	11	a
A	5	10	b
e	6	9	c
GND	7	8	d

DECIMAL FUNCT	LT	RBI	D C	B A	RBo	a	b	c	d	e	f	g	a b	c d	e f	g
	INPUTS					BI OUTPUTS (46,47)							OUTPUTS (48,49)			
0	H	H	L L	L L	H	ON	ON	ON	ON	ON	ON	OFF	H H	H H	H H	L
1	H	X	L L	L H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	L H	H L	L L	L
2	H	X	L L	H L	H	ON	ON	OFF	ON	ON	OFF	ON	H H	L H	H L	L
3	H	X	L L	H H	H	ON	ON	ON	ON	OFF	OFF	ON	H H	H H	L L	H
4	H	X	L H	L L	H	OFF	ON	ON	OFF	OFF	ON	ON	L H	H L	L H	H
5	H	X	L H	L H	H	ON	OFF	ON	ON	OFF	ON	ON	H L	H H	L H	H
6	H	X	L H	H L	H	OFF	OFF	ON	ON	ON	ON	ON	L L	H H	H H	H
7	H	X	L H	H H	H	ON	ON	ON	OFF	OFF	OFF	OFF	H H	H L	L L	L
8	H	X	H L	L L	H	ON	ON	ON	ON	ON	ON	ON	H H	H H	H H	H
9	H	X	H L	L H	H	ON	ON	ON	OFF	OFF	ON	ON	H H	H L	L H	H
10	H	X	H L	H L	H	OFF	OFF	OFF	ON	ON	OFF	ON	L L	L H	H L	H
11	H	X	H L	H H	H	OFF	OFF	ON	ON	OFF	OFF	ON	L L	H H	L L	H
12	H	X	H H	L L	H	OFF	ON	OFF	OFF	OFF	ON	ON	L H	L L	L H	H
13	H	X	H H	L H	H	ON	OFF	OFF	ON	OFF	ON	ON	H L	L H	L H	H
14	H	X	H H	H L	H	OFF	OFF	OFF	ON	ON	ON	ON	L L	L H	H H	H
15	H	X	H H	H H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	L L	L L	L L	L
BI/RBo	X	X	X X	X X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	L L	L L	L L	L
RBI	H	L	L L	L L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	L L	L L	L L	L
LT	L	X	X X	X X	H	ON	ON	ON	ON	ON	ON	ON	H H	H H	H H	H

7450 DUAL 2-WIDE 2-INPUT AND-OR-INVERT-GATES

Vcc = 5V DOUA PORTI SI-SAU-NU EXPANDABILA CU 2 INTRRI

$Y = \overline{A.B + C.D + X}$; X = OUTPUT OF 7460

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
50	16	0,4	1,6	40	14	10,5	13	8	4	7,4
H50	20	0,5	2	50	29	6,5	6,8	6,2	8,2	15,2

$1Y = \overline{A.B + C.D + X}$

$2Y = \overline{A.B + C.D}$

1A	1	14	Vcc
2A	2	13	1B
2B	3	12	1$\overline{X}$
2C	4	11	1X
2D	5	10	1D
2Y	6	9	1C
GND	7	8	1Y

7451 AND-OR-INVERT GATES

Vcc = 5V 2 PORTI SI-SAU-NU CU 2/3 INTRARI

$1Y = 2Y = \overline{A.B + C.D}$ (51,H51,S51)

$1Y = \overline{A.B.C + D.E.F}$ (L51, LS51) $2Y = \overline{A.B + C.D}$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
51	16	0,4	1,6	40	14	10,5	13	8	4	7,4
H51	20	0,5	2	50	29	6,5	6,8	6,2	8,2	15,2
S51	20	1	2	50	27	3,5	3,5	3,5	8,2	13,6
L51	3,6	0,2	0,18	10	1,5	42	50	35	0,44	0,76
LS51	8	0,4	0,4	20	2,8	12	12	12,5	0,8	1,4

1A	1	1A	Vcc	14	Vcc
2A	2	2A	1C	13	1B
2B	3	2B	1B	12	
2C	4	2C	1F	11	
2D	5	2D	1E	10	1D
2Y	6	2Y	1D	9	1C
GND	7	GND	1Y	8	1Y

(L51,LS51 interior)

7452 EXPANDABLE 4-WIDE AND-OR GATES

Vcc = 5V POARTA SI-SAU EXPANDABILA

$Y = A.B + C.D.E + F.G + H.I + X$ (X = OUTPUTS 7461)

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} uA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
H52	20	0,5	2	50	87	10	10,6	9,2	20	15,2

$Y = A.B + C.D + E.F + G.H.I + X$

(varianta H52W - vezi interior)

A	1	A	B	14	Vcc
B	2	C	X	13	I
C	3	D	Y	12	H
D	4	Vcc	GND	11	G
E	5	E		10	F
	6	F	I	9	X
GND	7	G	H	8	Y

7453 EXPANDABLE 4-WIDE AND-OR-INVERT GATES

Vcc = 5V POARTA SI-SAU-NU EXPANDABILA

$Y = \overline{A.B + C.D + E.F + G.H + X}$ (53) X = OUTPUT 7460

$Y = \overline{A.B + C.D + E.F.G + H.I + X}$ (H53) X = OUTPUT 74H60;74H62

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
53	16	0,4	1,6	40	23	10,5	13	8	4	5,1
H53	20	0,5	2	50	41	6,6	7	6,2	7,1	9,4

(H53 in interior)

A	1	A	Vcc	14	Vcc
C	2	C	B	13	B
D	3	D	$\overline{X}$	12	$\overline{X}$
E	4	E	X	11	X
F	5	F	I	10	H
	6	G	H	9	G
GND	7	GND	Y	8	Y

7454 4-WIDE AND-OR-INVERT GATES

Vcc = 5V POARTA SI-SAU-NU

$Y = \overline{A.B + C.D + E.F + G.H}$ (54) $Y = \overline{A.B + C.D + E.F.G. + H.I}$ (H54)

$Y = \overline{A.B + C.D.E + F.G.H. + I.J}$ (L54,LS54)

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
54	16	0,4	1,6	40	23	10,5	13	8	4	5,1
H54	20	0,5	2	50	41	6,5	7	6,2	7,1	9,4
L54	3,6	0,2	0,18	10	2,5	42	50	35	0,39	0,6
LS54	8	0,4	0,4	20	4,5	12	12	12,5	0,8	1

54 H54 L54	Pin	Pin	L54 H54 54
AAA	1	14	Vcc
CCB	2	13	jBB
DDC	3	12	I
EED	4	11	H
FFE	5	10	GIH
GY	6	9	FHG
GND	7	8	YYY

7455 2-WIDE 4-INPUT AND-OR-INVERT GATES

Vcc = 5V POARTA SI-SAU-NU

$Y = \overline{A.B.C.D + E.F.G.H + X}$ (H55-EXPANDABLE;X = 74H62)

$Y = \overline{A.B.C.D + E.F.G.H}$ (L55;LS55)

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
L55	3,6	0,2	0,18	10	1,5	41	50	35	0,22	0,38
LS55	8	0,4	0,4	20	2,8	12	12	12,5	0,4	0,7
H55	20	0,5	2	50	30	6,7	7	6,5	4,5	7,5

H55 L55	Pin	Pin	L55 H55
A A	1	14	Vcc
B B	2	13	H H
C C	3	12	G G
D D	4	11	F F
X	5	10	E E
	6	9	$\overline{X}$
GND	7	8	Y Y

7460 DUAL 4-INPUT EXPANDERS

Vcc = 5V DOUA CIRCUITE DE EXPANDARE

X = A.B.C.D (conectat la 7423;7450;7453;7455)

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
60			1,6	40	4	2	2	2	1,2	2
H60			2	50	6	2,7	4,2	1,2	1,9	3

	Pin	Pin	
1A	1	14	Vcc
1B	2	13	1D
1C	3	12	$\overline{1X}$
2A	4	11	1X
2B	5	10	2X
2C	6	9	$\overline{2X}$
GND	7	8	2D

7461 TRIPLE 3-INPUT EXPANDERS

Vcc=5V TREI CIRCUITE DE EXPANDARE

X= A.B.C (X conectat la 74H52)

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
H61			2	50	13	2,4	4,2	0,6	11	5

1A	1	14	Vcc
1B	2	13	3C
1C	3	12	3B
2A	4	11	3A
2B	5	10	3X
2C	6	9	1X
GND	7	8	2X

7462 4 WIDE AND-OR EXPANDERS

Vcc=5V CIRCUIT SI-SAU DE EXPANDARE

X= A.B+C.D.E+F.G.H+i.j (X conectat la 74H50;74H53;74H55)

X= A.B.C+D.E+F.G+H.i.j (varianta H62w)

TIP 74			I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
H62			2	50	24	2,2	3,2	1,2	6	3,8

H62w	H62			H62	H62w
A	A	1	14	Vcc	C
D	B	2	13	j	B
E	C	3	12	i	X
V_{cc}	D	4	11	H	GND
F	E	5	10	G	$\overline{X}$
G	$\overline{X}$	6	9	F	j
H	GND	7	8	X	i

7463 HEX CURRENT-SENSING INTERFACE GATES

Vcc=5V SASE CIRCUITE DE INTERFATA

Y= A

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} µA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
LS63	8	0,4	50	200	40	21	27	15	8	-

1A	1	14	Vcc
1Y	2	13	6A
2Y	3	12	6Y
2A	4	11	5Y
3A	5	10	5A
3Y	6	9	4A
GND	7	8	4Y

4-2-3-2 INPUT AND-OR-INVERT GATES

7464 POARTA SI-SAU-NU

7465 POARTA SI-SAU-NU CU COLECTOR IN GOL V0H=5V

$Y = \overline{A.B.C.D+E.F+G.HI+j.K}$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CCH} mA	I_{CCL} mA
S64	20	1	2	50	39	3,5	3,5	3,5	7	8,5
S65	20	0,25	2	50	36	5,5	5	5,5	6	8,5

A	1	14	Vcc
E	2	13	D
F	3	12	C
G	4	11	B
H	5	10	K
i	6	9	j
GND	7	8	Y

7470 AND-GATED j-k POZITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Vcc = 5V BISTABIL CU SI PE INTRARILE j_k,DECLANSAT PE FRONT POZITIV,CU SET SI RESET

TIP 74	TACT	FRECV MHz	P/F-F mW	tSETUP ns	tHOLD ns	tpd ns	tpLH ns	tpHL ns
70	L-H	35	65	20↑	[illegible]↑	23	27	17

	1	14	Vcc
CLR	2	13	PR
j1	3	12	CK
j2	4	11	K2
$\overline{j}$	5	10	K1
$\overline{Q}$	6	9	$\overline{K}$
GND	7	8	Q

INPUTS					OUTPUTS	
PRSET	CLEAR	CLOCK	j	k	Q	$\overline{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↑	L	L	Qo	$\overline{Qo}$
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	$\overline{Qo}$	Qo
H	H	L	X	X	Qo	$\overline{Qo}$

$j = j1.j2.\overline{j}$

$k = k1.k2.\overline{k}$

7471 AND-OR-GATES j-K MASTER-SLAVE FLIP-FLOPS WITH PRESET

Vcc = 5V BISTABIL STAPIN-SCLAV CU SI-SAU PE INTRARILE j-K CU SET

TIP 74	TACT	FRECV MHz	P/F-F mW	tSETUP ns	tHOLD ns	tpd ns	tpLH ns	tpHL ns
H71	H-L	30	80	0↑	0↓	18	14	22
L71	H-L	3	3,8	0↑	0↓	42	35	60

INPUTS H71				OUTPUTS	
PRESET	CLCK	j	k	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Qo	$\overline{Qo}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	$\overline{Qo}$	Qo

j1A	1	14	Vcc
j1B	2	13	CK
j2A	3	12	K2B
j2B	4	11	K2A
PR	5	10	K1B
Q	6	9	K1A
GND	7	8	$\overline{Q}$

j = (j1A.j1B) + (j2A.j2B)

K = (K1A.K1B) + (K2A.K2B)

L71 AND-GATED R-S MASTER-SLAVE FLIP-FLOP WITH PRESET AND CLEAR

INPUTS L71					OUTPUTS	
PRESET	CLEAR	CLOCK	R	S	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Qo	$\overline{Qo}$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	*	*

	1	14	Vcc
CLR	2	13	PR
S1	3	12	CK
S2	4	11	R3
S3	5	10	R2
$\overline{Q}$	6	9	R1
GND	7	8	Q

R = R1.R2.R3

S = S1.S2.S3

* = configuratie nedeterminata

H* = configuratie nestabila

7472 AND-GATED j-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

Vcc = 5V BISTABIL j-K MASTER-SLAVE

TIP 74	TACT	FRECV MHz	P/F-F mW	t_{SETUP} ns	t_{HOLD} ns	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
72	H-L	20	50	0↑	0↓	20	16	25
H72	H-L	30	80	0↑	0↓	18	14	22
L72	H-L	3	3,8	0↑	0↓	42	35	60

INPUTS					OUTPUTS	
PRSET	CLEAR	CLCK	j	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Qo	$\overline{Qo}$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	$\overline{Qo}$	Qo

	1	14	Vcc
CLR	2	13	PR
j1	3	12	CK
j2	4	11	K3
j3	5	10	K2
$\overline{Q}$	6	9	K1
GND	7	8	Q

j = j1.j2.j3

R = R1.R2.R3

7473 DUAL j-K MASTER-SLAVE FLIP-FLOPS WITH CLEAR

Vcc = 5V DOUA BISTABILE j-K/M-S

TIP 74	TACT	FREC MHz	P/F-F mW	t_{SETUP} ns	t_{HOLD} ns	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
73	H-L	20	50	0↑	0↓	20	16	25
H73	H-L	30	80	0↑	0↓	18	14	22
L73	H-L	3	3,8	0↑	0↓	42	35	60
LS73A	H-L	45	20	20↓	0↓	15	15	15

1CK	1	14	1j
1CLR	2	13	$\overline{1Q}$
1K	3	12	1Q
Vcc	4	11	GND
2CK	3	10	2K
2CLR	2	9	2Q
2j	1	8	$\overline{2Q}$

INPUTS 73,H73,L73				OUTPUTS	
CLEAR	CLOCK	j	k	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Qo	$\overline{Qo}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	$\overline{Qo}$	Qo

INPUTS LS73A				OUTPUTS	
CLR	CLCK	j	k	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Qo	$\overline{Qo}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	$\overline{Qo}$	Qo
H	H	X	X	Qo	$\overline{Qo}$

7474 DUAL TIPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Vcc = 5V DOUA BISTABILE DE TIP D

TIP 74	TACT	FREC MHz	P mW	t_{SEUP} ns	t_{HOLD} ns	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
74	L-H	25	43	$20\uparrow$	$5\uparrow$	17	14	20
H74	L-H	43	75	$15\uparrow$	$5\uparrow$	11	8,5	13
L74	L-H	3	4	$50\uparrow$	$15\uparrow$	65	65	65
LS74A	L-H	33	10	$25\uparrow$	$5\uparrow$	19	13	25
S74	L-H	110	75	$3\uparrow$	$2\uparrow$	6	6	6
ALS74	L-H	50	12	$15\uparrow$	$0\uparrow$	10	8	12

1CLR	1	14	Vcc
1D	2	13	2CLR
1CK	3	12	2D
1PR	4	11	2CK
1Q	5	10	2PR
$1\overline{Q}$	6	9	2Q
GND	7	8	$2\overline{Q}$

INPUTS 74				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	X	Qo	$\overline{Qo}$

INPUT 75		OUTPUT	
D	E	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qo	$\overline{Qo}$

7475 4-BIT BISTABILE LATCHES

Vcc = 5V 4 BISTABILE D CU RETINERE

TIP 74	ENAB	FREC MHz	P mW	t_{SET} ns	t_{HOLD} ns	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
75	H	25	160	20	5	15	16	14
L75	H	3	80	40	10	30	32	28
LS75	H	33	32	20	5	12	15	9

$1\overline{Q}$	1	16	1Q
1D	2	15	2Q
2D	3	14	$2\overline{Q}$
ENABLE 3-4	4	13	ENABLE 1-2
Vcc	5	12	GND
3D	6	11	$3\overline{Q}$
4D	7	10	3Q
$4\overline{Q}$	8	9	4Q

7476 DUAL j-k FLIP-FLOPS WITH PRESET AND CLEAR

Vcc = 5V 2 BISTABILE j-k

TIP 74	TACT	FREC MHz	P mW	t_{SEUP} ns	t_{HOLD} ns	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
76	H-L	20	50	$0\uparrow$	$0\uparrow$	22	16	25
H76	H-L	30	80	$0\uparrow$	$0\uparrow$	18	14	22
LS76A	H-L	45	10	$20\downarrow$	$0\uparrow$	15	15	15

1CK	1	16	1K
1PR	2	15	1Q
1CLR	3	14	$1\overline{Q}$
1j	4	13	GND
Vcc	5	12	2K
2CK	6	11	2Q
2PR	7	10	$2\overline{Q}$
2CLR	8	9	2j

TABELUL DE STARI IDENTIC 7472

7477 **4-BIT BISTABILE LATCHES**

Vcc = 5V **PATRU BISTABILE D CU RETINERE**

TIP 74	TACT	FREC MHz	P mW	t_{SET} ns	t_{HOLD} ns	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
L77	H	3	80	40	10	30	32	28

1D	1	14	1Q
2D	2	13	2Q
ENABLE 3-4	3	12	ENABLE 1-2
Vcc	4	11	GND
3D	5	10	
4D	6	9	3Q
	7	8	4Q

TABELUL DE STARI IDENTIC 7475

7478 **DUAL j-k FLIP-FLOPS WITH PRESET,COMMON CLEAR,COMMON CLOCK**

Vcc = 5V **DOUA BISTABILE j-k**

TIP 74	TACT	FREC MHz	P mW	t_{SEUP} ns	t_{HOLD} ns	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
H78	H-L	30	80	0↑	0↓	18	14	22
L78	H-L	3	3,8	0↑	0↓	42	35	60
LS78A	H-L	45	20	20↓	0↓	15	15	15

L78	H78			H78	L78
CK	1K	1	14	Vcc	1K
1PR	1Q	2	13	1PR	1Q
1j	$\overline{1Q}$	3	12	CLR	$\overline{1Q}$
Vcc	1j	4	11	2j	GND
CLR	$\overline{2Q}$	5	10	2PR	2j
2PR	2Q	6	9	CK	$\overline{2Q}$
2K	GND	7	8	2K	2Q
LS78A					LS78A

TABELUL DE STARI IDENTIC 7472

7480 **GATED FULL ADDERS**

Vcc = 5V **SUMATOR COMPLECT**

TIP 74	I_{0L} mA	I_{0H} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	I_{CC} mA
80	16/8	0,4/0,2	1,6	15	105	57	52	62	21

B*	1	14	Vcc
Bc	2	13	B2
Cn	3	12	B1
$\overline{Cn+1}$	4	11	Ac
S	5	10	A*
$\overline{S}$	6	9	A2
GND	7	8	A1

INPUTS			OUTPUTS		
Cn	B	A	$\overline{Cn+1}$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

$$A = \overline{Ac} + \overline{A^*} + A1.A2$$

$$B = \overline{Bc} + \overline{B^*} + B1.B2$$

7481 16-BIT RANDOM ACCESS MEMORIES

Vcc = 5V MEMORIE DE 16-BITI CU ACCES DIRECT CU S IN GOL

TIP 74	I_{OL} mA	I_{OH} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pHL} ns	t_{pLH} ns	t_{SR} ns
81	40	250	1,6/ 11	40/ 400	225	12,5	12	13	13

X1-X4 } ADDRESS
Y1-Y4 }

W-INPUT

S-OUTPUT

X3	1	14	X4
X2	2	13	WRITE 1
X1	3	12	SENSE 1
Vcc	4	11	SENSE 0
Y1	5	10	GND
Y2	6	9	WRITE 0
Y3	7	8	Y4

7482 2-BIT BINARY FULL ADDERS

Vcc = 5V SUMATOR COMPLECT PE 2 BITI

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
82	16	0,4	1,6/6,4	40/160	175	37,5	40	35

S1	1	14	A2
A1	2	13	B2
B1	3	12	S2
Vcc	4	11	GND
C0	5	10	C2
	6	9	
	7		

7483 4-BIT BINARY FULL ADDERS WITH FAST CARRY

Vcc = 5V SUMATOR BINAR PE 4 BITI CU TRANSPORT RAPID

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
83	16	0,8	1,6	40	330	16	16	16
LS83A	8	0,4	0,8	40	95	15,5	16	15

A4	1	16	B4
S3	2	15	S4
A3	3	14	C4
B3	4	13	C0
Vcc	5	12	GND
S2	6	11	B1
B2	7	10	A1
A2	8	9	S1

7484 16-BIT RANDOM ACCESS MEMORIES

Vcc = 5V MEMORIE CU ACCES DIRECT PE 16 BITI

TIP 74	I_{OL} mA	I_{OH} µA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	t_{SR} ns
84	40	250	1,6/11	40/400	225	12,5	12	13	13

X1-X4 } ADDRESS
Y1-Y4 }

W1 = W1(A).W1(B)

W0 = W0(A).W0(B)

W-INPUT

S-OUTPUT WITH OPEN COLLECTOR

X4	1	16	1(A)WRITE
X3	2	15	1(B)WRITE
X2	3	14	1SENCE
X1	4	13	0SENCE
Vcc	5	12	GND
Y1	6	11	0(A)WRITE
Y2	7	10	0(B)WRITE
Y3	8	9	Y4

7485 4-BIT MAGNITUDE COMPARATORS

Vcc = 5V COMPARATOR PE 4 BITI

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
85	16	0,4	1,6/4,8	40/160	275	21	23	20
L85	3,6	0,2	0,18/0,54	10/30	16	82	90	75
LS85	8	0,4	0,4/1,2	20/60	52	25	27	23
S85	20	1	2/6	50/150	550	11	12	11'

	Pin	Pin	
B3	1	16	Vcc
INPUTS A<B	2	15	A3
INPUTS A=B	3	14	B2
INPUTS A>B	4	13	A2
OUTS A>B	5	12	A1
OUTS A=B	6	11	B1
OUTS A<B	7	10	A0
GND	8	9	B0

WORD LENGTH	NR. OF PK.	85	L85	LS85	S85
1-4 BITS	1	23 ns	90 ns	24 ns	11 ns
5-24	2-6	46 ns	180ns	48 ns	22 ns
25-120	8-31	69 ns	270ns	72 ns	33 ns

7486 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

Vcc = 5V PATRU PORTI SAU-EXCLUSIV CU 2 INTRARI

$Y = A \oplus B$

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns	$P_{cc/p}$ mW
86	16	0,8	1,6	40	150	14	16	12	38
L86	3,6	0,2	0,36	20	19	55	62	47	4,75
LS86	8	0,4	0,8	40	30,5	14	16	12	7,6
S86	20	1	2	50	250	7	7	6,5	63

	Pin	Pin	
1A	1	14	Vcc
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

7487 4-BIT TRUE/COMPLEMENT,ZERO/ONE ELEMENTS

Vcc = 5V

TIP 74	I_{OL} mA	I_{OH} mA	I_{iL} mA	I_{iH} µA	P_{cc} mW	t_{pd} ns	t_{pLH} ns	t_{pHL} ns
H87	20	1	2	50	270	17	17	17

	Pin	Pin	
C	1	14	Vcc
A1	2	13	A4
Y1	3	12	Y4
	4	11	
A2	5	10	A3
Y2	6	9	Y3
GND	7	8	B

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

7488 **256-BIT READ-ONLY MEMORIES (ROM)**

Vcc = 5V 32 x 8 BIT WORDS OPEN COLLECTOR OUTPUTS

7488

D01	1	16	Vcc
D02	2	15	CS
D03	3	14	ADE
D04	4	13	ADD
D05	5	12	ADC
D06	6	11	ADB
D07	7	10	ADA
GND	8	9	D08

7489

ADA	1	16	Vcc
$\overline{ME}$	2	15	ADB
$\overline{WE}$	3	14	ADC
DI1	4	13	ADD
$\overline{D01}$	5	12	DI4
DI2	6	11	$\overline{D04}$
$\overline{D02}$	7	10	DI3
GND	8	9	$\overline{D03}$

7489 **64-BIT READ/WRITE MEMORIES**

Vcc = 5V 16 x 4 BIT WORDS

7490 **DECADE COUNTER**

Vcc = 5V DIVIDE-BY-TWO AND DIVIDE-BY-FIVE

NUMARATOR DECADIC (DIVIZOR DE 2 SI 5)

7491 **8-BIT SHIFT REGISTERS**

Vcc = 5V REGISTRU DE DEPLASARE PE 8 BITI

TIP 74	TACT	FREC MHz	t_{pH} ns	t_{pLH} ns	P_{CC} ns
91A	L-H	18	24	27	175
L91	L-H	6,5	55	100	17,5
LS91	L-H	18	24	27	60

INPUTS AT_{tn}		OUTPUTS AT_{tn+8}	
A	B	QH	$\overline{QH}$
H	H	H	L
L	X	L	H
X	L	L	H

	1	14	$\overline{QH}$
	2	13	QH
	3	12	INPUT A
	4	11	INPUT B
Vcc	5	10	GND
	6	9	CLOCK
	7	8	

7492 **DIVIDE-BY-TWELVE COUNTERS**

NUMARATOR DIVIZOR PRIN 12

7493 **4-BIT BINARY COUNTERS**

Vcc = 5V NUMARATOR BINAR DE 4 BITI

90A, L90, LS90

INTB	1	14	INTA
R0(1)	2	13	
R0(2)	3	12	QA
	4	11	QD
Vcc	5	10	GND
R9(1)	6	9	QB
R9(2)	7	8	QC

92A, LS92

INTB	1	14	INTA
	2	13	
	3	12	QA
	4	11	QB
Vcc	5	10	GND
R0(1)	6	9	QC
R0(2)	7	8	QD

93A, LS93

INTB	1	14	INTA
R0(1)	2	13	
R0(2)	3	12	QA
	4	11	QD
Vcc	5	10	GND
	6	9	QB
	7	8	QD

L93

R0(1)	1	14	INTA
R0(2)	2	13	QA
	3	12	QD
Vcc	4	11	GND
	5	10	QC
	6	9	QB
	7	8	INTB

90A,L90,LS90

NR.	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

QA conectat la int.B

90A,L90,LS90

NR.	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

QD conectat la int.A

92A,LS92

NR.	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

QA conectat la int.B

93A,L93,LS93

NR	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

QA conectat la int B

TIP 74	TACT	FREC MHz	Pcc mW	IiL mA	IiH µA	tpLH ns	tpHL ns	tSETUP ns
90A	H-L	42	145	4,8	120	32	34	25
L90	H-L	6	20	1,08	60	230	230	
LS90	H-L	42	45	3,2	80	32	34	25
92A	H-L	42	130	4,8	120	32	34	25
LS92	H-L	42	45	3,2	80	32	34	25
93A	H-L	42	130	3,2	80	46	46	25
L93	H-L	6	16	0,36	20	280	280	
LS93	H-L	42	45	2,4	80	46	46	25

RESET/COUNT FUNCTION TABLE
90A,LS90,L90

RESET INPUTS				OUTPUTS			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

RESET/COUNT FUNCTION TABLE
92A,LS92,93A,LS93,L93

RESET		OUTPUTS			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

7494 4-BIT-SHIFT REGISTER/DUAL ASYNCHRONOUS PRESET

Vcc = 5V REGISTRU DE DEPLASARE PE 4 BITI CU DOUA INTRARI ASINCRONE DE PUNERE PE "1"

PRESET				INTERN	INTERN.PRESET				INPUTS			INTERN OUT			OUT.
PE1	P1i	PE2	P2i	PRESET i	A	B	C	D	CLR	CLK	SER	QA	QB	QC	QD
L	X	L	X	H	H	H	H	H	H	X	X	L	L	L	L
L	X	X	L	H	L	L	L	L	L	X	X	H	H	H	H
X	L	L	X	H	H	H	H	H	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
X	L	X	L	H	L	H	L	H	L	L	X	H	Q_{B0}	H	Q_{D0}
H	H	X	X	L(act.)	H	H	H	H	L	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
X	X	H	H	L(act.)	H	H	H	H	L	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}

P1i = int.P1A,P1B,P1C,P1D Q_{A0},Q_{B0},Q_{C0},Q_{D0} - nivel QA,QB,QC,QD inainte CLOCK

P2i = int.P2A,P2B,P2C,P2D   QAn,QBn,QCn,QDn - nivel QA,QB,QC,QD dupa CLOCK

i = internal A,B,C,D

P1A	1	16	P2A
P1B	2	15	PE2
P1C	3	14	P2B
P1D	4	13	P2C
Vcc	5	12	GND
PE1	6	11	P2D
SER.IN.	7	10	CLEAR
CLOCK	8	9	OUT.

REG. DE DEPLASARE DE TIP INTRARE SERIE-IESIRE SERIE

INTRARE PARALELA-IESIRE SERIE

TIP	FREC	Pcc	IiH	IiL	t_{pLH}	t_{pHL}	t_{SETUP}
74	MHz	mW	uA	mA	ns	ns	ns
94	10	175	160	6,4	25	25	35

7495 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

REGISTRU DE DEPLASARE PE 4 BITI CU ACCES PARALEL

TIP	FREC	Pcc	I_{iH}	I_{iL}	t_{pLH}	t_{pHL}	tSU	thold
74	MHz	mw	µa	ma	ns	ns	ns	ns
95A	36	195	80	3,2	18	21	15	0
L95	5	19	20	0,36	115	125	100	120
LS95A	36	65	20	0,4	18	21	20	10

INPUTS							OUTPUTS			
MODE CNTRL	CLOCKS 2(L)	1(R)	SER	PARALLEL A	B	C	D	QA	QB	QC	QD
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	QB↑	QC↑	Qd↑	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

SER	1	14	Vcc
A	2	13	QA
B	3	12	QB
C	4	11	QC
D	5	10	QD
MODE	6	9	CLCK R
GND	7	8	CLCK L

input (A, B, C, D)

7496 5-BIT SHIFT REGISTERS
REGISTRU DE DEPLASARE PE 5 BITI

TIP 74	FREC MHz	Pcc mw	I_{iH} µA	I_{iL} mA	t_{pLH} ns	t_{pHL} ns	t_{SU} ns
96	10	240	200	8	25	25	30
L96	5	120	100	4	50	50	100
LS96	25	60	100	2	25	25	30

	Pin	Pin	
CLOCK	1	16	CLEAR
A	2	15	Q_A
B	3	14	Q_B
C	4	13	Q_C
Vcc	5	12	GND
D	6	11	Q_D
E	7	10	Q_E
PRESET ENABLE	8	9	SERIAL IN

INPUT CLR	EN	PRESET A	B	C	D	E	CLK	SER	OUTPUT QA	QB	QC	QD	QE
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

SYNCRONOUS 6-BIT BINARY RATE MULTIPLIERS
NUMARATOR PROGRAMABIL PE 6 BITI

TIP 74	FREC MHz	Pcc mw	I_{iH} µA	I_{iL} mA	t_{SU} ns	t_h ns
97	32	345	80	3,2	25	20

	Pin	Pin	
B	1	16	Vcc
E	2	15	D
F	3	14	C
A	4	13	CLR
Z	5	12	CASC.
Y	6	11	ENABLE IN
ENABLE OUT.	7	10	STROBE
GND	8	9	CLOCK

$$f_{out} = \frac{M.f_{in}(CLOCK)}{64}$$

unde : $M = F.2^5 + E.2^4 + D.2^3 + C.2^2 + B.2^1 + A.2^0$

INPUTS CLR	EN IN	STB	BINARY RATE F	E	D	C	B	A	NR CLK	CAS	OUTPUTS NR. PULSES Y	Z	EN OUT
H	X	H	X	X	X	X	X	X	X	H	L	H	H
L	L	L	L	L	L	L	L	L	64	H	L	H	1
L	L	L	L	L	L	L	L	H	64	H	1	1	1
L	L	L	L	L	L	L	H	L	64	H	2	2	1
L	L	L	L	L	L	H	L	L	64	H	4	4	1
L	L	L	L	L	H	L	L	L	64	H	8	8	1
L	L	L	L	H	L	L	L	L	64	H	16	16	1
L	L	L	H	L	L	L	L	L	64	H	32	32	1
L	L	L	H	H	H	H	H	H	64	H	63	63	1
L	L	L	H	H	H	H	H	H	64	L	H	63	1
L	L	L	H	L	H	L	L	L	64	H	40	40	1

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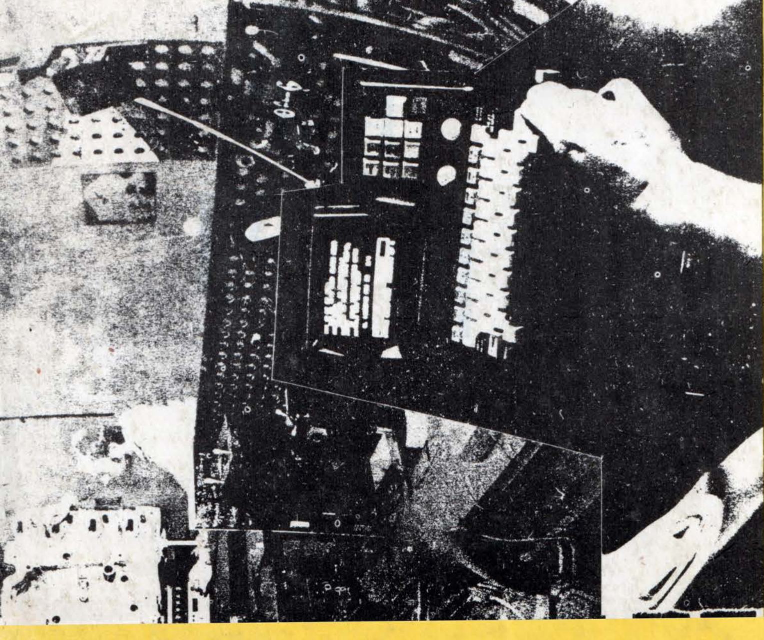
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